Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims (with markings):

1. (Currently Amended) A circuit~~method~~ fo~~r~~ ~~implementing~~ a filter comprises:~~ing of a transmission line of one or more segments with fixed propagation delays for forward signal propagation or for feedback signal propagation.~~

~~For forward signal propagation, an input signal connected to a transmission line consisting of one or more segments with each segment providing its own fixed propagation delay. The nodes connecting said transmission line segments, the node at the input to the first delay segment and the node at the output of the last delay segment are connected to the inputs of one or more transconductance elements. When there are multiple outputs of the said transconductance elements, the said outputs are connected together to form the sum of the currents.~~

a forward transmission delay line configured to have at least one forward transmission line delay element;

an input signal coupled to the at least one forward transmission line delay element for time-delaying the input signal by corresponding at least one forward delay time of the at least one forward transmission line delay element;

a first termination impedance coupled to an output of the forward transmission delay line for terminating the forward transmission delay line;

at least one input of the at least one forward transconductance element coupled to at least one output of the at least one forward transmission line delay element for multiplying at least one time-delayed input signal by at least one forward filter coefficient and for converting at least one multiplied time-delayed input signal to at least one forward current;

the at least one forward transconductance element configured to have corresponding at least one forward transconductance;

an input of a no-delay transconductance element coupled to the input signal for multiplying the input signal by a no-delay filter coefficient and for converting the input signal to a no-delay current;

the no-delay transconductance element configured to have a no-delay transconductance;

an output of the no-delay transconductance element and at least one output of the at least one forward transconductance element coupled together to form a current summing node for summing the at least one forward current into a summed current;

a transimpedance element coupled to the current summing node and configured to convert the summed current to an output voltage signal;

~~For feedback signal propagation, a method for implementing a filter comprising of an input signal connected to a transconductance element, whose output is connected to a shunt impedance element and to the input of a transmission line consisting of one or more segments with each segment providing its own fixed propagation delay. The nodes connecting the said transmission line segments and the node at the output of the last delay segment are connected to the inputs of one or more transconductance elements. When there are multiple outputs of the said transconductance elements, the said outputs are connected together to form the sum of the currents for feeding back to the input of the said transmission line.~~

a feedback transmission delay line configured to have at least one feedback transmission line delay element;

the output voltage signal coupled to the at least one feedback transmission line delay element for time-delaying the output voltage signal by corresponding at least one feedback delay time of the at least one feedback transmission line delay element;

a second termination impedance coupled to an output of the feedback transmission delay line for terminating the feedback transmission delay line; at least one feedback transconductance element coupled to at least one output of the at least one feedback transmission line delay element for multiplying at least one time-delayed output signal by at least one feedback filter coefficient and converting at least one multiplied time-delayed output signal to at least one feedback current;

the at least one feedback transconductance element configured to have corresponding at least one feedback transconductance; and

at least one output of the at least one feedback transconductance element coupled together at the current summing node for summing the at least one feedback current into the summed current.

~~The said impedance element can be replaced by a serial transimpedance element whose input is connected to the output of the transconductors and whose output is connected to the input of the transmission line.~~

~~The said forward signal propagation transmission line filter and the said feedback signal propagation transmission line filter each separately or combined can form the implementation of a filter with any type of network, lattice, or cascaded filter structures.~~

2. (Currently Amended) The circuit~~method~~ of claim 1 wherein the input signal is single ended or differential and the output signals is~~are~~ single ended or differential.
~~Wherein the number of transmission line segments are an integer, N, with N > 1;~~
~~Wherein the number of transconductance elements are an integer, M, with M >1;~~
~~Wherein the analog filter implementation is fixed, programmable, or adaptive.~~

3. (Currently Amended) The circuit~~method~~ of claim 1 wherein the said transmission line ~~segments~~delay elements configured as waveguides, microstrip lines, stripline transmission lines, coaxial lines or two-wire lines are implemented on an integrated circuit device, off an integrated circuit chip, on a ~~silicon or other~~ semiconductor substrates, on a~~the~~ package substrate~~,~~ or on a printed circuit ~~PCB~~ board (PCB~~,~~ ).~~as co-planar waveguides, as microstrip lines, as stripline transmission lines or any other known transmission line types.~~

4. (Currently Amended) The circuit~~method~~ of claim 1 wherein each of the said transmission line delay elements ~~segments can have its own~~ has a fixed or a programmable delay time~~value~~.

5. (Currently Amended) The ~~method~~circuit of claim 1 wherein a~~the~~ number of the at least one forward transmission line delay elements and a number of the at least one feedback transmission line delay ele~~se~~gments are ~~can be~~ fixed or programmable.

6. (Currently Amended) The ~~method~~circuit of claim 1 wherein each of the at least one forward transconductance elements and the at least one feedback transconductance element is~~are~~ implemented as a transconductance amplifiers, as a multistage voltage amplifiers, resistors, or a combination of resistors and voltage amplifiers.

7. (Currently Amended) The ~~method~~circuit of claim 1 wherein each of the transconductances of the no-delay, the at least one forward and the at least one feedback transconductance elements

is configured to haveare implemented as a fixed valuetransconductance, aas programmable valuetransconductance, or anas adaptively controlled valuetransconductance.

8. (Cancelled)The method of claim 1 wherein the impedance element comprises a resistor or resistors, capacitors, inductors or resistor, capacitor and inductor combination networks.

9. (Currently Amended) The method circuit of claim 1 wherein each of the first and the second termination impedances element is configured to have ahas fixed matched or mismatched impedance in response to a system filter requirement specification. , programmable impedance, or adaptively adjustable impedance.

10. (Currently Amended) The method circuit of claim 1 wherein the transimpedance element comprises a transimpedance amplifier configured for ahas fixed transimpedance, a programmable transimpedance, or an adaptively controlled transimpedance.

11. (Currently Amended) The circuitmethod of claim 1 further comprises inputwherein matching impedancecomponents elements configured for matching to are placed at the corresponding inputs of the said transconductance elements.; wherein the impedance element comprises a resistor or resistors, capacitors, inductors or resistor, capacitor and inductor combination networks; wherein the impedance element has fixed impedance, programmable impedance, or adaptively adjustable impedance

12. (Cancelled) The method of claim 1 further comprises an impedance element whose input is connected to the outputs of said transconductance elements , wherein the impedance element comprises a resistor or resistors, capacitors, inductors or resistor, capacitor and inductor combination networks; wherein the impedance element has fixed impedance, programmable impedance, or adaptively adjustable impedance.

13. (Cancelled) ~~The method of claim 1 wherein the outputs of said transconductance elements are connected together at the input of a transimpedanceamplifier wherein the transimpedance amplifier has fixed transimpedance, programmable transimpedance, or adaptively adjustable transimpedance.~~

14. (Cancelled) ~~The method of claim 1 wherein the transmission line is terminated by an impedance element, wherein the said impedance element is a network of resistors, capacitors, and inductor elements; wherein the impedance element has fixed impedance, programmable impedance, or adaptively adjustable impedance.~~

15. (Currently Amended) The circuit~~method~~ of claim 1 ~~used in a feed forward equalization (FFE) filter, a decision feedback equalization (DFE) filter, a finite impulse response (FIR) filter,~~wherein the analog filter is configured as ~~a~~ an infinite impulse response (IIR) filter for ~~, an~~ equalizing the input signal in disk drives, ~~ation filter, adaptive equalization filter, equalization filter for~~ optical ~~channels~~, serial chip-to-chip, serial backplane ~~equalization filter for electrical channels, a radio frequency filter for radio reception,~~ high speed network, or ~~a~~ radio frequency communication systems.~~filter for radio transmission~~.

16. (Currently Amended) A circuit~~method fo~~f~~r implementing~~ a finite impulse response (FIR) filter comprises:~~ing of a transmission line of one or more segments with fixed propagation delays for forward signal propagation or for feedback signal propagation.~~

~~For forward signal propagation, an input signal connected to a transmission line consisting of one or more segments with each segment providing its own fixed propagation delay. The nodes connecting said transmission line segments, the node at the input to the first delay segment and the node at the output of the last delay segment are connected to the inputs of one or more transconductance elements. When there are multiple outputs of the said transconductance elements, the said outputs are connected together to form the sum of the currents.~~

a forward transmission delay line configured to have at least one forward transmission line delay element;

an input signal coupled to the at least one forward transmission line delay element for time-delaying the input signal by corresponding at least one forward delay time of the at least one forward transmission line delay element;

a termination impedance element coupled to an output of the forward transmission delay line for terminating the forward transmission delay line;

at least one input of the at least one forward transconductance element coupled to at least one output of the at least one forward transmission line delay element for multiplying at least one time-delayed input signal by at least one forward filter coefficient and for converting at least one multiplied time-delayed input signal to at least one forward current;

the at least one forward transconductance element configured to have corresponding at least one forward transconductance;

an input of a no-delay transconductance element coupled to the input signal for multiplying the input signal by a no-delay filter coefficient and for converting the input signal to a no-delay current;

the no-delay transconductance element configured to have a no-delay transconductance;

an output of the no-delay transconductance element and at least one output of the at least one forward transconductance element coupled together to form a current summing node for summing the at least one forward current into a summed current;

a transimpedance element coupled to the current summing node and configured to convert the summed current to an output voltage signal.

~~For feedback signal propagation, a method for implementing a filter comprising of an input signal connected to a transconductance element, whose output is connected to a shunt impedance element and to the input of a transmission line consisting of one or more segments with each segment providing its own fixed propagation delay. The nodes connecting the said transmission line segments and the node at the output of the last delay segment are connected to the inputs of one or more transconductance elements. When there are multiple outputs of the said transconductance elements, the said outputs are connected together to form the sum of the currents for feeding back to the input of the said transmission line.~~

~~The said impedance element can be replaced by a serial transimpedance element whose input is connected to the output of the transconductors and whose output is connected to the input of the transmission line.~~

~~The said forward signal propagation transmission line filter and the said feedback signal propagation transmission line filter each separately or combined can form the implementation of a filter with any type of network, lattice, or cascaded filter structures.~~

17. (New) The circuit of claim 1 further comprises a control circuit coupled to the no-delay transconductance element, the at least one forward transconductance element and the at least one feedback transconductance element for tuning the said transconductance elements.

18. (New) The circuit of claim 2 further comprises a control circuit coupled to the no-delay transconductance element, the at least one forward transconductance element and the at least one feedback transconductance element for tuning the said transconductance elements.

19. (New) The circuit of claim 1 wherein an absolute value of the no-delay filter coefficient is equal to the transconductance of the no-delay transconductance element, at least one forward absolute value of the at least one forward filter coefficient is equal to the corresponding at least one forward transconductance of the at least one forward transconductance element, and at least one feedback absolute value of the at least one feedback filter coefficient is equal to the corresponding at least one feedback transconductance of at least one transconductance element.

20. (New) The circuit of claim 2 wherein an absolute value of the no-delay filter coefficient is equal to the transconductance of the no-delay transconductance element and at least one forward absolute value of the at least one forward filter coefficient is equal to the corresponding at least one forward transconductance of the at least one forward transconductance element.

21. (New) The circuit of claim 1 wherein the no-delay transconductance element is removed for a zero no-delay filter coefficient specification.

22. (New) The circuit of claim 1 wherein the analog filter is configured for filtering the input signal of frequency from 1 GHz to an order of 100 GHz.

23. (New) The circuit of claim 1 wherein each of the no-delay transconductance element, the at least one forward transconductance element and the at least one feedback transconductance element further comprises:
a differential gate terminal of a differential transistor pair coupled to the input signal wherein the input signal is differential;
a differential source terminal of the differential transistor pair coupled to a ground or a negative power supply via a differential current source; and
a variable resistor coupled between the differential source terminal.

24. (New) The circuit of claim 23 wherein the variable resistor configured to tune the transconductance further comprises:
a fixed resistor coupled to at least one switched resistor in series,
at least one switch coupled to the at least one switched resistor,
a closed state of the at least one switch configured to short out the at least one switched resistor for decreasing a total resistance of the variable resistor, and
an open state of the at least one switch configured to switch in the at least one switched resistor for increasing the total resistance of the variable resistor.

25. (New) The circuit of claim 23 wherein the transimpedance element is configured to include a load resistor pair coupled between the differential drain terminal and a power supply.

26. (New) The circuit of claim 23 wherein a positive signal of the input signal is coupled to a negative terminal of the differential gate terminal and a negative signal of the input signal is coupled to a positive terminal of the differential gate terminal.

27. (New) The circuit of claim 1 wherein the filter configured as a one-tap filter further comprises:
A circuit of a one-tap filter comprises:
a first transconductance element coupled to an input signal for multiplying the input signal by a first filter coefficient and for converting the multiplied input signal to a first current;

an input of a transimpedance element coupled to an output of the first transconductance element for converting the first current to a voltage signal;

a first terminal of a transmission line delay element coupled to the first voltage signal for time delaying the voltage signal;

a time-delayed voltage signal coupled to a second terminal of the transmission line delay element;

a termination impedance coupled to the second terminal of the transmission line delay element:

a second transconductance element coupled to the time-delayed voltage signal for multiplying the time-delay voltage signal by a second filter coefficient and for converting the multiplied time-delay voltage signal to a second current; and

an output of the second transconductance element coupled to the output of the first transconductance element to form a summing node at the input of the transimpedance element for summing the second current into the first current.

28. (New) The circuit of claim 27 wherein the filter is configured to be one of a high pass filter or a low pass filter.

29. (New) A backplane system comprises:

a buffer coupled to a first terminal of a backplane channel for buffering a transmit signal;

a buffered transmit voltage signal propagating through the backplane channel and degraded by a backplane channel low pass filtering; and

an input terminal of an analog equalizer coupled to a second terminal of the backplane channel ;

wherein the analog equalizer configured as a high pass filter for equalizing the degraded buffered transmit voltage signal further comprises:

a forward transmission delay line configured to include at least one transmission line delay elements for time delaying the degraded buffered transmit signal,

a termination impedance to terminate the transmission delay line,

the at least one transmission line delay elements coupled to at least one transconductance amplifier for multiplying at least one time delayed degraded buffered transmit voltage signal by corresponding at least one filter coefficient and for converting the at least one time delayed degraded buffered transmit voltage signal to at least one forward current,

a no-delay transconductance element coupled to the buffered transmit signal for multiplying the degraded buffered transmit signal by corresponding a no-delay filter coefficient and for converting the degraded buffered transmit voltage signal to a no-delay current,

at least one output of the at least one transconductance element and an output of the no-delay transconductance element coupled together to form a summing node for summing the at least one current and the no-delay current into a summed current,

a transimpedance amplifier coupled to the summing node for converting the summed current into an equalized voltage signal;

a feedback transmission delay line configured to have at least one feedback transmission line delay element;

the equalized voltage signal coupled to the at least one feedback transmission line delay element for time-delaying the equalized voltage signal by corresponding at least one feedback delay time of the at least one feedback transmission line delay element;

a second termination impedance coupled to an output of the feedback transmission delay line for terminating the feedback transmission delay line; at least one feedback transconductance element coupled to at least one output of the at least one feedback transmission line delay element for multiplying at least one time-delayed equalized voltage signal by at least one feedback filter coefficient and converting at least one multiplied time-delayed equalized voltage signal to at least one feedback current;

the at least one feedback transconductance element configured to have corresponding at least one feedback transconductance; and

at least one output of the at least one feedback transconductance element coupled together at the current summing node for summing the at least one feedback current into the summed current.

30. (New) The backplane system of claim 30 wherein the analog equalizer configured as a FIR filter comprises:

a forward transmission delay line configured to include at least one transmission line delay elements for time delaying the degraded buffered transmit signal,

a termination impedance to terminate the transmission delay line,

the at least one transmission line delay elements coupled to at least one transconductance amplifier for multiplying at least one time delayed degraded buffered transmit voltage signal by

corresponding at least one filter coefficient and for converting the at least one time delayed degraded buffered transmit voltage signal to at least one forward current,

a no-delay transconductance element coupled to the buffered transmit signal for multiplying the degraded buffered transmit signal by corresponding a no-delay filter coefficient and for converting the degraded buffered transmit voltage signal to a no-delay current,

at least one output of the at least one transconductance element and an output of the no-delay transconductance element coupled together to form a summing node for summing the at least one current and the no-delay current into a summed current,

a transimpedance amplifier coupled to the summing node for converting the summed current into an equalized voltage signal.

Listing of Claims (clean version):

1. (Currently Amended) A circuit of a filter comprises:

a forward transmission delay line configured to have at least one forward transmission line delay element;

an input signal coupled to the at least one forward transmission line delay element for time-delaying the input signal by corresponding at least one forward delay time of the at least one forward transmission line delay element;

a first termination impedance coupled to an output of the forward transmission delay line for terminating the forward transmission delay line;

at least one input of the at least one forward transconductance element coupled to at least one output of the at least one forward transmission line delay element for multiplying at least one time-delayed input signal by at least one forward filter coefficient and for converting at least one multiplied time-delayed input signal to at least one forward current;

the at least one forward transconductance element configured to have corresponding at least one forward transconductance;

an input of a no-delay transconductance element coupled to the input signal for multiplying the input signal by a no-delay filter coefficient and for converting the input signal to a no-delay current;

the no-delay transconductance element configured to have a no-delay transconductance;

an output of the no-delay transconductance element and at least one output of the at least one forward transconductance element coupled together to form a current summing node for summing the at least one forward current into a summed current;

a transimpedance element coupled to the current summing node and configured to convert the summed current to an output voltage signal;

a feedback transmission delay line configured to have at least one feedback transmission line delay element;

the output voltage signal coupled to the at least one feedback transmission line delay element for time-delaying the output voltage signal by corresponding at least one feedback delay time of the at least one feedback transmission line delay element;

a second termination impedance coupled to an output of the feedback transmission delay line for terminating the feedback transmission delay line; at least one feedback transconductance element coupled to at least one output of the at least one feedback transmission line delay element for multiplying at least one time-delayed output signal by at least one feedback filter coefficient and converting at least one multiplied time-delayed output signal to at least one feedback current;
the at least one feedback transconductance element configured to have corresponding at least one feedback transconductance; and
at least one output of the at least one feedback transconductance element coupled together at the current summing node for summing the at least one feedback current into the summed current.

2. (Currently Amended) The circuit of claim 1 wherein the input signal is single ended or differential and the output signal is single ended or differential.

3. (Currently Amended) The circuit of claim 1 wherein the said transmission line delay elements configured as waveguides, microstrip lines, stripline transmission lines, coaxial lines or two-wire lines are implemented on an integrated circuit device, off an integrated circuit chip, on a semiconductor substrate, on a package substrate or on a printed circuit board (PCB).

4. (Currently Amended) The circuit of claim 1 wherein each of the said transmission line delay elements has a fixed or a programmable delay time.

5. (Currently Amended) The circuit of claim 1 wherein a number of the at least one forward transmission line delay elements and a number of the at least one feedback transmission line delay elements are fixed or programmable.

6. (Currently Amended) The circuit of claim 1 wherein each of the at least one forward transconductance element and the at least one feedback transconductance element is implemented as a transconductance amplifier, as a multistage voltage amplifier, resistors, or a combination of resistors and voltage amplifiers.

7. (Currently Amended) The circuit of claim 1 wherein each of the transconductances of the no-delay, the at least one forward and the at least one feedback transconductance elements is configured to have a fixed value, a programmable value, or an adaptively controlled value.

8. (Cancelled)

9. (Currently Amended) The circuit of claim 1 wherein each of the first and the second termination impedances is configured to have a matched or mismatched impedance in response to a system filter requirement specification.

10. (Currently Amended) The circuit of claim 1 wherein the transimpedance element comprises a transimpedance amplifier configured for a fixed transimpedance, a programmable transimpedance, or an adaptively controlled transimpedance.

11. (Currently Amended) The circuit of claim 1 further comprises input matching impedance elements configured for matching to the corresponding inputs of the said transconductance elements.

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Currently Amended) The circuit of claim 1 wherein the analog filter is configured as an infinite impulse response (IIR) filter for equalizing the input signal in disk drives, optical , serial chip-to-chip, serial backplane high speed network, or radio frequency communication systems..

16. (Currently Amended) A circuit of a finite impulse response (FIR) filter comprises:

a forward transmission delay line configured to have at least one forward transmission line delay element;

an input signal coupled to the at least one forward transmission line delay element for time-delaying the input signal by corresponding at least one forward delay time of the at least one forward transmission line delay element;

a termination impedance element coupled to an output of the forward transmission delay line for terminating the forward transmission delay line;

at least one input of the at least one forward transconductance element coupled to at least one output of the at least one forward transmission line delay element for multiplying at least one time-delayed input signal by at least one forward filter coefficient and for converting at least one multiplied time-delayed input signal to at least one forward current;

the at least one forward transconductance element configured to have corresponding at least one forward transconductance;

an input of a no-delay transconductance element coupled to the input signal for multiplying the input signal by a no-delay filter coefficient and for converting the input signal to a no-delay current;

the no-delay transconductance element configured to have a no-delay transconductance;

an output of the no-delay transconductance element and at least one output of the at least one forward transconductance element coupled together to form a current summing node for summing the at least one forward current into a summed current;

a transimpedance element coupled to the current summing node and configured to convert the summed current to an output voltage signal.

17. (New) The circuit of claim 1 further comprises a control circuit coupled to the no-delay transconductance element, the at least one forward transconductance element and the at least one feedback transconductance element for tuning the said transconductance elements.

18. (New) The circuit of claim 2 further comprises a control circuit coupled to the no-delay transconductance element, the at least one forward transconductance element and the at least one feedback transconductance element for tuning the said transconductance elements.

19. (New) The circuit of claim 1 wherein an absolute value of the no-delay filter coefficient is equal to the transconductance of the no-delay transconductance element, at least one forward absolute value of the at least one forward filter coefficient is equal to the corresponding at least one forward transconductance of the at least one forward transconductance element, and at least one feedback absolute value of the at least one feedback filter coefficient is equal to the corresponding at least one feedback transconductance of at least one transconductance element.

20. (New) The circuit of claim 2 wherein an absolute value of the no-delay filter coefficient is equal to the transconductance of the no-delay transconductance element and at least one forward absolute value of the at least one forward filter coefficient is equal to the corresponding at least one forward transconductance of the at least one forward transconductance element.

21. (New) The circuit of claim 1 wherein the no-delay transconductance element is removed for a zero no-delay filter coefficient specification.

22. (New) The circuit of claim 1 wherein the analog filter is configured for filtering the input signal of frequency from 1 GHz to an order of 100 GHz.

23. (New) The circuit of claim 1 wherein each of the no-delay transconductance element, the at least one forward transconductance element and the at least one feedback transconductance element further comprises:
a differential gate terminal of a differential transistor pair coupled to the input signal wherein the input signal is differential;
a differential source terminal of the differential transistor pair coupled to a ground or a negative power supply via a differential current source; and
a variable resistor coupled between the differential source terminal.

24. (New) The circuit of claim 23 wherein the variable resistor configured to tune the transconductance further comprises:
a fixed resistor coupled to at least one switched resistor in series,
at least one switch coupled to the at least one switched resistor,

a closed state of the at least one switch configured to short out the at least one switched resistor for decreasing a total resistance of the variable resistor, and

an open state of the at least one switch configured to switch in the at least one switched resistor for increasing the total resistance of the variable resistor.

25. (New) The circuit of claim 23 wherein the transimpedance element is configured to include a load resistor pair coupled between the differential drain terminal and a power supply.

26. (New) The circuit of claim 23 wherein a positive signal of the input signal is coupled to a negative terminal of the differential gate terminal and a negative signal of the input signal is coupled to a positive terminal of the differential gate terminal.

27. (New) The circuit of claim 1 wherein the filter configured as a one-tap filter further comprises:

A circuit of a one-tap filter comprises:

a first transconductance element coupled to an input signal for multiplying the input signal by a first filter coefficient and for converting the multiplied input signal to a first current;

an input of a transimpedance element coupled to an output of the first transconductance element for converting the first current to a voltage signal;

a first terminal of a transmission line delay element coupled to the first voltage signal for time delaying the voltage signal;

a time-delayed voltage signal coupled to a second terminal of the transmission line delay element;

a termination impedance coupled to the second terminal of the transmission line delay element:

a second transconductance element coupled to the time-delayed voltage signal for multiplying the time-delay voltage signal by a second filter coefficient and for converting the multiplied time-delay voltage signal to a second current; and

an output of the second transconductance element coupled to the output of the first transconductance element to form a summing node at the input of the transimpedance element for summing the second current into the first current.

28. (New) The circuit of claim 27 wherein the filter is configured to be one of a high pass filter or a low pass filter.

29. (New) A backplane system comprises:

a buffer coupled to a first terminal of a backplane channel for buffering a transmit signal;

a buffered transmit voltage signal propagating through the backplane channel and degraded by a backplane channel low pass filtering; and

an input terminal of an analog equalizer coupled to a second terminal of the backplane channel ;

wherein the analog equalizer configured as a high pass filter for equalizing the degraded buffered transmit voltage signal further comprises:

a forward transmission delay line configured to include at least one transmission line delay elements for time delaying the degraded buffered transmit signal,

a termination impedance to terminate the transmission delay line,

the at least one transmission line delay elements coupled to at least one transconductance amplifier for multiplying at least one time delayed degraded buffered transmit voltage signal by corresponding at least one filter coefficient and for converting the at least one time delayed degraded buffered transmit voltage signal to at least one forward current,

a no-delay transconductance element coupled to the buffered transmit signal for multiplying the degraded buffered transmit signal by corresponding a no-delay filter coefficient and for converting the degraded buffered transmit voltage signal to a no-delay current,

at least one output of the at least one transconductance element and an output of the no-delay transconductance element coupled together to form a summing node for summing the at least one current and the no-delay current into a summed current,

a transimpedance amplifier coupled to the summing node for converting the summed current into an equalized voltage signal;

a feedback transmission delay line configured to have at least one feedback transmission line delay element;

the equalized voltage signal coupled to the at least one feedback transmission line delay element for time-delaying the equalized voltage signal by corresponding at least one feedback delay time of the at least one feedback transmission line delay element;

a second termination impedance coupled to an output of the feedback transmission delay line for terminating the feedback transmission delay line; at least one feedback transconductance element coupled to at least one output of the at least one feedback transmission line delay element for multiplying at least one time-delayed equalized voltage signal by at least one feedback filter coefficient and converting at least one multiplied time-delayed equalized voltage signal to at least one feedback current;

the at least one feedback transconductance element configured to have corresponding at least one feedback transconductance; and

at least one output of the at least one feedback transconductance element coupled together at the current summing node for summing the at least one feedback current into the summed current.

30. (New) The backplane system of claim 30 wherein the analog equalizer configured as a FIR filter comprises:

a forward transmission delay line configured to include at least one transmission line delay elements for time delaying the degraded buffered transmit signal,

a termination impedance to terminate the transmission delay line,

the at least one transmission line delay elements coupled to at least one transconductance amplifier for multiplying at least one time delayed degraded buffered transmit voltage signal by corresponding at least one filter coefficient and for converting the at least one time delayed degraded buffered transmit voltage signal to at least one forward current,

a no-delay transconductance element coupled to the buffered transmit signal for multiplying the degraded buffered transmit signal by corresponding a no-delay filter coefficient and for converting the degraded buffered transmit voltage signal to a no-delay current,

at least one output of the at least one transconductance element and an output of the no-delay transconductance element coupled together to form a summing node for summing the at least one current and the no-delay current into a summed current,

a transimpedance amplifier coupled to the summing node for converting the summed current into an equalized voltage signal.